Drain-to-gate field engineering for improved frequency response of GaN-based HEMTs

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A B S T R A C T

We report on a novel approach for designing high-frequency AlGaN/GaN HEMTs based on gate-drain field engineering. This approach uses a drain-connected field controlling electrode (FCE). The devices with gate-to-FCE separation of 0.5–0.7 μm exhibit much smaller frequency behavior degradation with drain bias at least up to 30 V and yield RF gain and output power improvement up to ~2 times compared to conventional devices. These results show that the FCE is a powerful technique of improving the high-frequency, high power performance of GaN HEMTs at high drain biases.

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1. Introduction

High electron density, high breakdown field, and high electron saturation velocity of GaN-based semiconductors have led to high power and efficiency of GaN microwave amplifiers up to 10 GHz [2] with demonstrated potential of operating at higher frequencies [3]. However, the highest achieved cutoff frequencies are significantly lower than those estimated from the electron transit time under the gate with the peak 2D electron velocities. The upper bound for the BET cutoff frequency can be estimated as $f_T = v_s S / 2 \pi L_{eff}$, where $v_s$ is electron saturation velocity in the channel and $L_{eff}$ is the effective gate length. For the predicted electron peak velocities up to $2.5 \times 10^7$ cm/s [4], a GaN HEMT with 100 nm gate length should achieve ~400 GHz cutoff frequency. However, the best value reported by Palacios et al. for a 100 nm gate was $f_T = 153$ GHz which is less than half of the expected performance [5]. For a more aggressive design with a 30 nm gate length, Higashiwaki et al. reported $f_T = 181$ GHz [3]. The estimated $f_T$ for such a short channel device should exceed 1 THz. Even though parasitics might limit the cutoff frequency [6], the major reason for the discrepancy between expected and observed $f_T$ values was recently attributed to a very large extension of the space charge into the drain-to-gate spacing of GaN HEMTs [7]. This phenomenon is particularly important for high power devices, where much higher drain biases are required and both effective electron velocity and effective channel length extension can be significantly different from those at relatively low drain biases, where the cutoff frequency as a performance parameter is typically reported. Under typical operation conditions, neglecting the parasitic resistances, the saturation drain current of a short channel HFET can be described using the gradual channel approximation [8]:

$$I_D = C(V_{gs} - V_T) v_s W < q n_{so} v_s W$$

where $I_D$ is drain current, $C$ is the gate-to-channel capacitance, $q$ is elementary charge, $v_s$ is the effective electron saturation velocity, $V_{gs}$ is the gate bias, $V_T$ is the channel potential at the edge of the velocity saturation region under the gate (the point under the gate closest to the drain where gradual channel approximation is still valid), $n_{so}$ is the low field carrier concentration in the ungated region of the device. The lateral electric field further increases throughout the portion of the gated channel where velocity is saturated. As a result, the lateral field at the drain edge of the gate is much higher than the saturation electric field (and increases with the drain bias). The high lateral electric field penetrates into the

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ungated gate-to-drain spacing, resulting in velocity saturation there as well. The current continuity condition means that the sheet carrier concentration in the saturated channel remains constant equal to \( C \left( V_{gs} - V_{th} - V_{ds} \right) / q \) and smaller than equilibrium (low field) concentration (see Eq. (1)). Hence, it cannot fully compensate positive polarization charge that induces the 2DEG. This positive charge increases with the drain bias because of the increase in the high field region extension resulting in additional gate-to-drain capacitance. Alternatively, this effect can be explained as an extension of the effective gate length.

The effect of such extension depends on the device surface potential in the drain-to-gate spacing as follows. Outside the device gate area, the Gradual Channel approximation gives \( q \cdot n_{surf}(x) = C \left( V_{surf}(x) - V_{th} - V_{ch}(x) \right) \) where \( n_{surf}(x) \) is lateral coordinate dependent sheet carrier concentration, \( V_{surf} \) is local surface potential, and \( V_{ch} \) is corresponding channel potential. \( V_{th} \) has a meaning of threshold voltage in the ungated region. Let \( V_{ch} - V_{surf} \) be a difference between surface and channel potential outside the gate that corresponds to low field sheet carrier concentration \( n_{surf} \). From Eq. (1) it can be seen that within high field region extension in the device gate-to-drain spacing,

\[
V_{surf}(x) - V_{ch}(x) < V_{ch} - V_{surf}
\]

(2)

As seen, the surface potential with respect to channel potential within high field region extension is lower than that in the equilibrium. Therefore, externally lowering the surface potential leads to the high field region extension. Conventional gate connected or source-connected field plates reduce the peak field but increase the length of the velocity saturation region, leading to a further extension of this region into the gate-to-drain spacing [9,10] and further reducing \( f_t \). Interestingly enough, SiN passivation has a similar effect [5], since it makes the surface potential distribution between gate and drain more uniform, thus increasing the extension of the depletion region into the gate-to-drain spacing.

As suggested in [7], using the field controlled electrode (FCE) connected to the drain, one should achieve the suppression of the gate length extension with increasing drain bias by squeezing the velocity saturation region into a shorter spacing between the FCE and the gate. This should improve the device bias-frequency performance. In contrast to conventional field plate, the drain-connected electrode results in a more uniform field distribution in gate-drain region. Therefore, this field controlling electrode (FCE) can be used for any high voltage device design, which requires the maximum voltage drop uniformity over the device active area.

In this study, we fabricated a variety of devices with FCEs with different FCE-gate spacing and investigated the effect of FCEs on device cutoff frequency as function of the drain bias.

2. Device design and fabrication

The device epilayer structures for this study were grown by migration enhanced metal-organic chemical vapor deposition (MEMOCVD) [11] on insulating 4H-SiC substrates. A thin low temperature AlN is followed by 1.5 \( \mu \)m undoped GaN channel layer and capped by 22 nm Si-doped \( \text{Al}_{0.3}\text{Ga}_{0.7}\text{N} \) layer. The Hall 2D gas sheet resistance was 253 Q/sq. HEMT devices were fabricated by a similar process described in [12]. The fabrication process started with chlorine-based inductively coupled plasma (ICP) etching for mesa isolation. After that, source and drain ohmic contacts were defined by UV optical lithography, formed by e-beam evaporation of Ti/AI/Ti/Au metal stack and annealing at 800 °C in Nitrogen ambient for 1 min. Sub-micron gates with the length \( L_G = 300–500 \)\( \text{nm} \) were realized by e-beam patterning and Ni/Au deposition. Then a 100 nm thick Si\( \text{N}_3 \) was deposited by plasma enhanced chemical vapor deposition (PECVD), patterned by optical lithography and etched away from the contacts. FCEs were also patterned by e-beam lithography and formed by Ti/Au deposition. Length of the FCE was \( L_{FCE} = 0.5 \)\( \mu \)m for all devices, while gate-to-FCE distance \( D_{G-FCE} \) was varied from 0.3 \( \mu \)m to 0.7 \( \mu \)m. FCEs were connected to the drain by thin stripes. Devices had two gate fingers of 50 \( \mu \)m each giving 100 \( \mu \)m of total device width. Fingers had U-shape configuration. Schematics of cross-section and top view and SEM picture of the fabricated devices are shown in the Fig. 1. Conventional HEMTs without FCEs were also fabricated on the same wafers for comparison purposes. Extensive simulated electric field and electron velocity distribution characteristics in the devices similar to the fabricated ones can be found in Ref. [7].

3. Device performance and discussion

The fabricated HEMTs with and without FCEs exhibited peak drain currents of 0.8 A/mm at zero gate bias, and the threshold voltage of around \( V_{th} = -4.5 \) V. The small signal s-parameters and large signal RF power at 2 GHz were measured using the Maury automated tuning system at the gate bias corresponding to the peak \( f_t \), \( V_{ds} = -3.5 \) V. The pad associated parasitic parameters removal procedure utilized the small signal characteristics of a

![Fig. 1. (a) Schematics of cross-section and top view and (b) SEM picture of the fabricated device.](Image)
deeply pinched-off HEMT without FCE at zero drain bias using a method similar to the one proposed earlier by Oxley et al. [13].

Fig. 2 shows the drain bias dependence of normalized $f_t$ for the fabricated devices with FCE-to-gate separations of 0.5 and 0.7 $\mu$m and without FCEs. At relatively low drain bias of $V_{DS} = 15$ V, the cutoff frequency for all devices is almost same, slightly exceeding 60 GHz. As the drain bias is increased to 30 V, $f_t$ of a conventional HEMT drops significantly to 54.3 GHz. HEMTs with $D_{G-FCE} = 0.7$ $\mu$m also exhibited some, much less pronounced, decrease of $f_t$ with increasing drain bias. On the other hand, HEMTs with $D_{G-FCE} = 0.5$ $\mu$m did not show any $f_t$ decrease and even reached $f_t$ of 63.1 GHz at $V_{DS} = 30$ V. Bringing the field controlling electrode closer to the gate, to $D_{G-FCE} = 0.3$ $\mu$m, resulted in the $f_t$ drop down to $\sim$53 GHz, due to a higher gate-to-drain fringing capacitance, although no further cutoff frequency reduction with drain bias was observed as well.

In order to determine the effective gate length, we first estimated the electron velocity in the channel using the measured high-frequency data. The results were analyzed based on the gate length dependence of the measured $f_t$ data. We assumed that varying the gate length in the range from 0.3 to 0.5 $\mu$m does not significantly affect the gate length extension for both devices with and without FCE. With this assumption, in the plot of the reciprocal cutoff frequency versus the gate length, the slope of the line gives the effective saturation velocity value, $v_s$, while the $x$-axis intercept is equal to the value of channel extension. Thus, assuming that $L_{GEFF} = L_g + \Delta L_g + L_e$ where $\Delta L_g$ is the channel extension beyond the gate towards the drain side, we estimated $L_{GEFF}$ and $v_s$. By comparing the measurement results for the devices with different gate lengths, we extracted both electron velocity and channel extension. The procedure yields the effective saturation velocity value, $v_s = 1.3 \times 10^7$ cm/s. This value is lower than the values of $1.6 \times 10^7$ cm/s reported in [14] and $1.86 \times 10^7$ cm/s reported in [15], since the measurements in [13–14] were performed under conditions corresponding to the highest achievable channel velocity. In contrast, our results are obtained for a high drain bias relevant to high power GaN-based HFETs.

The variation of the extracted effective gate length for different drain biases is shown in Fig. 2. As seen, different devices exhibit significant variations in the gate length extension, which we attribute to the non-uniformity of surface conditions. However, the devices with $D_{G-FCE} = 0.7$ $\mu$m demonstrated a much smaller increase in the effective gate length. The devices with $D_{G-FCE} = 0.5$ $\mu$m did not show any significant gate length variation, in agreement to the results of Fig. 1. $D_{G-FCE} = 0.5$ $\mu$m was nearly the optimum gate-to-FCE distance for the fabricated devices (see Fig. 2). For a smaller gate-to-FCE distance (e.g., $D_{G-FCE} = 0.3$ $\mu$m), the gate-to-FCE parasitic coupling counter balances the benefit of a more uniform field provided by FCE, and can also reduce the device breakdown voltage. The extracted variation in the effective gate length with the drain bias for both conventional and FCE device is in full agreement with our previous simulations [7].

The RF power was measured in the CW mode, optimizing the load impedance for maximum output power near saturation individually for each device. The RF power measurements confirmed that the device power performance benefited from the more uniform electric field and improved saturation velocity. Compared to the devices without the FCE, the saturation RF power in the FCE devices was 1.4–1.8 times higher. At 2 GHz, the FCE devices demonstrated the large signal gain of about 5 dB higher than conventional devices. A similar power increase was previously reported for the devices having gate- or source-connected field plates [9,10,16] but at the expense of the $f_t$ reduction. A similar increase of the output RF power is observed by all devices having FCE, independently of the gate-to-FCE distance (see Fig. 3). This is in agreement with the results reported in [16] that showed that the RF power improvement by a field plate is linked not only to the electric field reduction but also to the effects of passivation (see Fig. 4).

The proposed design should also reduce the current collapse and improve reliability, since the FCE reduces the maximum electric field in the gate-to-drain spacing because of a more uniform electric field distribution.
4. Conclusions

In conclusion, we presented a novel design of high-frequency AlGaN/GaN HEMTs based on engineering the electric field in the gate-to-drain spacing utilizing a drain-connected field controlling electrode. FCE confined the high field into a smaller space and hence reduced the extension of effective gate length at high drain biases. Therefore, we conclude that the FCE is a powerful approach for improving the high-frequency, high power performance of GaN HEMTs at high drain biases and opens a way to a novel high-frequency device design using field engineering in the gate–drain region. This approach will be especially useful for designing GaN-based HEMTs operating at 26 GHz and higher.

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References